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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/549,291	09/16/2005	Junko Iwanaga	071971-0361	8090
53080	7590	07/07/2009		
MCDERMOTT WILL & EMERY LLP			EXAMINER	
600 13TH STREET, NW				LIN, JOHN
WASHINGTON, DC 20005-3096			ART UNIT	PAPER NUMBER
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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/549,291	IWANAGA ET AL.	
	<b>Examiner</b>	<b>Art Unit</b>	
	JOHN LIN	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) Responsive to communication(s) filed on 07 April 2009.  
 2a) This action is **FINAL**.                    2b) This action is non-final.  
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) Claim(s) 1-4,6-8 and 12-22 is/are pending in the application.  
 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
 5) Claim(s) \_\_\_\_\_ is/are allowed.  
 6) Claim(s) 1-4,6-8 and 12-22 is/are rejected.  
 7) Claim(s) \_\_\_\_\_ is/are objected to.  
 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) The specification is objected to by the Examiner.  
 10) The drawing(s) filed on \_\_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.  
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
 a) All    b) Some \* c) None of:  
 1. Certified copies of the priority documents have been received.  
 2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- 1) Notice of References Cited (PTO-892)  
 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)  
 3) Information Disclosure Statement(s) (PTO/SB/08)  
 Paper No(s)/Mail Date \_\_\_\_\_.  
 4) Interview Summary (PTO-413)  
 Paper No(s)/Mail Date. \_\_\_\_\_.  
 5) Notice of Informal Patent Application  
 6) Other: \_\_\_\_\_.

## DETAILED ACTION

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

**Claims 1, 2, 4 and 12** are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,288,431, granted to “**Iwasa**,” in view of U.S. Patent 4,996,574, granted to “**Shirasaki**,” in view of U.S. Patent 4,356,211, granted to “**Riseman**.”

**Claim 1:** Iwasa discloses a semiconductor device, in Figs. 1 and 3D, comprising:

    a semiconductor substrate (1), the semiconductor substrate contains an impurity of a first conductive type;

    a source region and a drain region (22), each of which contains an impurity of a second conductive type;

    a semiconductor FIN (11) provided between the source region and the drain region, the semiconductor FIN having an upper surface and both side surfaces;

    a gate insulating film (12) provided on the upper surface and the both side surfaces of the semiconductor FIN; and

    a gate electrode (21) formed directly on the gate insulating film (column 11, line 49 – column 12, line 10).

Iwasa appears not to explicitly disclose a semiconductor substrate in which a trench is formed; source and drain regions buried in the trench, and a semiconductor FIN buried in part of the trench.

Shirasaki, however, discloses forming a semiconductor FIN and source and drain regions in a trench of a substrate is a suitable alternative to forming them on a substrate (Figs 9 and 10).

Since forming a semiconductor FIN and source and drain regions in a trench of a substrate is a suitable alternative to forming them on a substrate, it would therefore have been obvious to modify Iwasa to have formed the semiconductor FIN and the source and drain regions in a trench of the substrate. Forming the semiconductor FIN and the source and drain regions in a trench of the substrate, the gate electrode would then have a planar portion extending from the upper surface of the semiconductor FIN, over the upper portion of the trench, to portion of the semiconductor substrate in which the trench is not formed, wherein the gate electrode has in the trench, termination structures extending toward a bottom of the trench along both sides of the semiconductor FIN.

Iwasa in view of Shirasaki appears not to explicitly disclose a channel stopper formed in a region located at a bottom portion of the trench in the semiconductor substrate and containing an impurity of the first conductive type at a high concentration than that in the semiconductor substrate.

Riseman, however, discloses forming a channel stopper 22 below a trench 20, the channel stopper having an impurity of the same conductivity type as the substrate

and at a concentration higher than the substrate to avoid short circuiting (Fig. 9; column 4, lines 14-24).

To avoid short circuiting therefore it would have been obvious to modify Iwasa in view of Shirasaki to have a channel stopper formed in a region located at a bottom portion of the trench in the semiconductor substrate and containing an impurity of the first conductive type at a high concentration than that in the semiconductor substrate.

**Claim 2:** Iwasa discloses the semiconductor FIN is made of Si (column 12, line 35-36).

**Claim 4:** Shirasaki discloses the gate electrode is provided on the gate insulating film so as to extend over the semiconductor substrate; the gate insulating film is provided on part of the semiconductor substrate in which the trench is not formed as well as the both side surfaces and the upper surface of the semiconductor FIN; and part of the gate insulating film located on the part of the semiconductor substrate in which the trench is not formed is interposed between the semiconductor substrate and the gate electrode (Fig. 10A).

**Claim 12:** Iwasa discloses the upper surface of the gate electrode has an even surface (Fig. 1).

**Claim 3** is rejected under 35 U.S.C. 103(a) as being unpatentable over Iwasa in view of Shirasaki in view of Riseman as applied to claims 1, 2, 4 and 12 above, and further in view of U.S. Patent 4,868,632 granted to **“Hayashi.”**

**Claim 3:** Iwasa in view of Shirasaki in view of Riseman discloses all the limitations of claim 1. Iwasa in view of Shirasaki in view of Riseman appear not to explicitly disclose an isolation insulating film is further provided between part of the semiconductor substrate located in a side wall portion of the trench and part of the gate electrode located over the side wall of the semiconductor FIN and an insulating film is further provided between part of the semiconductor substrate in which the trench is not formed and the gate electrode.

Hayashi, however, discloses a gate insulating film with three layers (106, 017, 108; Fig. 1; column 3, lines 15-28) to better insulated the gate from the rest of the transistor.

To better insulated the gate from the rest of the transistor therefore it would have been obvious to modify Iwasa in view of Shirasaki in view of Riseman to have provided an isolation insulating film between part of the semiconductor substrate located in a side wall portion of the trench and part of the gate electrode located over the side wall of the semiconductor FIN and to have provided an insulating film between part of the semiconductor substrate in which the trench is not formed and the gate electrode.

**Claims 6, 8 and 13** are rejected under 35 U.S.C. 103(a) as being unpatentable over Iwasa in view of Shirasaki in view of Riseman in view of U.S. Patent 7,163,851, granted to **“Abadeer.”**

**Claim 6:** Iwasa discloses a field-effect transistor, Figs. 1 and 3D, including a semiconductor substrate (1), a source region and a drain region (22) each of which

contains an impurity of the same conductive type, a semiconductor FIN (11) provided between the source region and the drain region, the semiconductor FIN having an upper surface and both side surfaces, a gate insulating film (12) provided on the upper surface and the both side surfaces of the semiconductor FIN, and a gate electrode (21) formed directly on the first gate insulating film (column 11, line 49 – column 12, line 10).

Iwasa appears not to explicitly disclose a semiconductor substrate in which a trench is formed; source and drain regions buried in the trench, and a semiconductor FIN buried in part of the trench.

Shirasaki, however, discloses forming a semiconductor FIN and source and drain regions in a trench of a substrate is a suitable alternative to forming them on a substrate (Figs 9 and 10).

Since forming a semiconductor FIN and source and drain regions in a trench of a substrate is a suitable alternative to forming them on a substrate, it would therefore have been obvious to modify Iwasa to have formed the semiconductor FIN and the source and drain regions in a trench of the substrate. Forming the semiconductor FIN and the source and drain regions in a trench of the substrate, the gate electrode would then have a planar portion extending from the upper surface of the semiconductor FIN, over the upper portion of the trench, to portion of the semiconductor substrate in which the trench is not formed, wherein the gate electrode has in the trench, termination structures extending from the upper surface of the semiconductor FIN toward a bottom of the trench along the both sides of the semiconductor FIN.

Iwasa in view of Shirasaki appears not to explicitly disclose a channel stopper formed in a region located at a bottom portion of the trench in the semiconductor substrate and containing an impurity of the first conductive type at a high concentration than that in the semiconductor substrate.

Riseman, however, discloses forming a channel stopper 22 below a trench 20, the channel stopper having an impurity of the same conductivity type as the substrate and at a concentration higher than the substrate to avoid short circuiting (Fig. 9; column 4, lines 14-24).

To avoid short circuiting therefore it would have been obvious to modify Iwasa in view of Shirasaki to have a channel stopper formed in a region located at a bottom portion of the trench in the semiconductor substrate and containing an impurity of the first conductive type at a high concentration than that in the semiconductor substrate.

Iwasa in view of Shirasaki in view of Riseman appears not to explicitly disclose two field-effect transistors on the same substrate.

Abadeer, however, discloses a FinFet integrated with another FET to increase device density (column 1, line 7 – column 2, line 4).

To increase device density therefore it would have been obvious to modify Iwasa in view of Shirasaki to have provided the field-effect transistor of Lee on the same substrate to increase device density.

**Claim 8:** Shirasaki discloses the gate electrode is provided on the gate insulating film so as to extend over the semiconductor substrate; the gate insulating film is provided on part of the semiconductor substrate in which the trench is not formed as

well as the both side surfaces and the upper surface of the semiconductor FIN; and part of the gate insulating film located on the part of the semiconductor substrate in which the trench is not formed is interposed between the semiconductor substrate and the gate electrode (Fig. 10A).

**Claim 13:** Iwasa discloses the upper surface of the gate electrode has an even surface (Fig. 1).

**Claim 7** is rejected under 35 U.S.C. 103(a) as being unpatentable over Iwasa in view of Shirasaki in view of Riseman in view of Abadeer as applied to claims 6, 8 and 13 above, and further in view of Hayashi.

**Claim 7:** Iwasa in view of Shirasaki in view of Lee in view of Abadeer discloses all the limitations of claim 6. Iwasa in view of Shirasaki appear not to explicitly disclose an isolation insulating film formed between part of the semiconductor substrate located in a side wall portion of the trench and part of the gate electrode provided over the side wall of the semiconductor FIN and an insulating film formed between the semiconductor substrate in which the trench is not formed and the first get electrode.

Hayashi, however, discloses a gate insulating film with three layers (106, 017, 108; Fig. 1; column 3, lines 15-28) to better insulated the gate from the rest of the transistor.

To better insulated the gate from the rest of the transistor therefore it would have been obvious to modify Iwasa in view of Shirasaki to have formed an isolation insulating film between part of the semiconductor substrate located in a side wall portion of the

trench and part of the gate electrode provided over the side wall of the semiconductor FIN and to have formed an insulating film between the semiconductor substrate in which the trench is not formed and the first get electrode.

**Claims 14, 16-18 and 20-22** are rejected under 35 U.S.C. 103(a) as being unpatentable over Iwasa in view of Riseman.

**Claim 14:** Iwasa discloses a semiconductor device, Figs. 1 and 3D, comprising:

- a semiconductor region (region of 1 between element 23) of a conductive type having a main surface;
- a trench (area between element 23) formed in the semiconductor region and having a bottom portion;
- a semiconductor FIN (11) formed in the trench;
- source and drain regions (22) formed so as to be buried in the trench and connected to the semiconductor FIN;
- a gate insulating film (12) formed so as to cover both side surfaces of the semiconductor FIN; and
- a gate electrode (21) formed on the gate insulating film and having in the trench, termination structures extending toward the bottom portion of the trench along the both sides of the semiconductor FIN(column 11, line 49 – column 12, line 10).

Iwasa appears not to explicitly disclose a heavily doped impurity region of the conductive type formed in the semiconductor region at the bottom portion of the trench and under the semiconductor FIN and the source and drain regions.

Riseman, however, discloses forming a heavily doped impurity region 22 of a conductive type formed in the semiconductor region at a bottom portion of a trench 20 to avoid short circuiting (Fig. 9; column 4, lines 14-24).

To avoid short circuiting therefore it would have been obvious to modify Iwasa to have a heavily doped impurity region of the conductive type formed in the semiconductor region at the bottom portion of the trench. Iwasa in view of Riseman would then disclose the heavily doped impurity region is formed under the semiconductor FIN and the source and drain regions.

**Claim 16:** Iwasa discloses a first insulating film (portion of 24 under element 11) formed between the semiconductor FIN and the semiconductor region (Fig. 1).

**Claim 17:** Iwasa discloses a second insulating film (portion of 24 under element 22) formed between the source and drain regions and the semiconductor region (Fig. 1).

**Claim 18:** Iwasa discloses a third insulating film (23) formed on the semiconductor region and the first insulating film, wherein the gate electrode is formed on the third insulating film (Fig. 1).

**Claim 20:** Iwasa discloses the gate electrode does not entirely cover the side surfaces of the semiconductor FIN (region 22 of element 11).

**Claim 21:** Iwasa discloses a source-LDD region (22a) and a drain-LDD region (22a) are formed in the semiconductor FIN (Fig. 8C; column 17, lines 48-62).

**Claim 22:** Iwasa discloses an insulating film (24) formed between the semiconductor FIN and the semiconductor region and formed between the semiconductor region and the source and drain regions (Fig. 1).

**Claim 15** is rejected under 35 U.S.C. 103(a) as being unpatentable over Iwasa in view of Riseman as applied to claims 14, 16-18 and 20-22 above, and further in view of U.S. Patent 6,770,516, granted to “Wu.”

**Claim 15:** Iwasa in view of Riseman discloses all the limitations of claim 14. Iwasa in view of Riseman appears not to explicitly disclose the semiconductor device has a double-gate structure, and a part of the gate insulating film formed above the semiconductor FIN has a larger thickness than a part of the gate insulating film formed in the side surfaces of the semiconductor FIN.

Wu, however, discloses a semiconductor FIN 3 having an insulating film 4 formed above the FIN having a thickness larger than an insulating film 7 formed on the side surfaces of the FIN to provide protection for the FIN (Fig. 4B; column 3, lines 20-65).

To protect the semiconductor FIN therefore it would have been obvious to modify Iwasa to have made a part of the gate insulating film formed above the semiconductor FIN have a larger thickness than a part of the gate insulating film formed in the side surfaces of the semiconductor FIN. Wu discloses this structure is a double-gate structure (column 3, lines 51-60).

**Claim 19** is rejected under 35 U.S.C. 103(a) as being unpatentable over Iwasa in view of Riseman as applied to claims 14,16-18 and 20-22 above, and further in view of Shirasaki.

**Claim 19:** Iwasa in view of Riseman discloses all the limitations of claim 14. Iwasa in view of Riseman appears not to explicitly disclose each width of the source and drain regions is larger than that of semiconductor FIN.

Shirasaki, however, discloses a semiconductor FIN 31c having a width smaller than the width of the source and drain regions 31a and 31b to provide more surface area to form contacts for the source and drain regions (Fig. 10).

To provide more surface area to form contacts for the source and drain regions therefore it would have been obvious to modify Iwasa to have each width of the source and drain regions larger than that of semiconductor FIN.

### ***Response to Arguments***

Applicant's arguments with respect to claims 1-4, 6-8 and 12-22 have been considered but are moot in view of the new ground(s) of rejection.

### ***Conclusion***

A shortened statutory period for reply to this Office Action is set to expire THREE MONTHS from the mailing date of this Office Action. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JOHN LIN whose telephone number is (571)270-1274. The examiner can normally be reached on M-F, 8AM-5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ken Parker can be reached on 571-272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Matthew E Warren/  
Primary Examiner, Art Unit 2815

/J. L./  
Examiner, Art Unit 2815